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TRANSMITTAL FORM

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Total Number of Pages in This Submission	41

Application No.	09/823,391
Filing Date	March 30, 2001
First Named Inventor	Monte J. Rhoads
Group Art Unit	2841
Examiner Name	D. Levi
Attorney Docket Number	42390P11044

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ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
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- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Basic Filing Fee
  - ☐ Declaration/POA
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Kerry D. Tweet, Reg. No. 45,959 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	March 6, 2003

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 320.00

Complete if Known	
Application Number	09/823,391
Filing Date	March 30, 2001
First Named Inventor	Monte J. Rhoads
Examiner Name	D. Levi
Group/Art Unit	2841
Attorney Docket No.	42390P11044

METHOD OF PAYMENT (check one)

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None
☐ Deposit Account

Deposit Account Number: 02-2666
Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments
☒ Charge any additional fee(s) required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims		- 58** =		X	=
Independent Claims		- 6 =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple Dependent claim, if not paid
1204	84	2204	42	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater, For Reissues, see below*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1404	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320.00
1403	280	2403	140	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	1809	375	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 320.00

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SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Kerry D. Tweet	Registration No. (Attorney/Agent)	45,959	Telephone	(503) 684-6200
Signature				Date	03/06/03

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Rhoads

Serial No.: 09/823,391

Filed: March 30, 2001

For: Riser Assembly and Method for Coupling Peripheral Cards to a Motherboard

Examiner: D. Levi

Group Art Unit: 2841

Attorney Docket No. 42.P11044

"Express Mail" mailing label number: EL625203306
Date of Deposit: March 4, 2003

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service on the date indicated above and that this paper or fee has been addressed to the Commissioner for Patents, Washington, D.C. 20231

Cindy C. Tsui 3/6/03 4/2/03
Signature Date

#22/Appeal Brief R.Ty

BRIEF ON APPEAL

COMMISSIONER FOR PATENTS
Washington, D.C. 20231
Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is in furtherance of the Notice of Appeal mailed on January 6, 2003, and received in the Patent Office on January 13, 2003. Pursuant to M.P.E.P. § 1206, the time period for filing this appeal brief expires on March 13, 2003, and this brief is filed by Express Mail pursuant to 37 C.F.R. § 1.10 prior to the expiration of this time period. The brief is submitted in triplicate in the format of 37 C.F.R. § 1.192(c), and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Intel Corporation of Santa Clara, California.

(2) RELATED APPEALS AND INTERFERENCES

Neither the appellant, the appellant's representative, nor the assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF THE CLAIMS

Claims 1-58 are pending in the application.

Claims 1-3, 5-14, 16-26, 28-46, 48-50, and 52-58 stand rejected, and claims 4, 15, 27, and 51 stand objected to.

The rejections of claims 1-3, 5-14, 16-26, 28-46, 48-50, and 52-58 are being appealed.

(4) STATUS OF AMENDMENTS

The application was filed on March 30, 2001, with claims 1-39. In an Office Action mailed January 29, 2002, claims 1-39 were subject to a requirement for restriction. In a response dated February 29, 2002, a provisional election was made, and the restriction requirement was traversed. In a subsequent Office Action mailed April 10, 2002, the restriction requirement was withdrawn.

In the Office Action of April 10, 2002, claims 1, 2, 5-8, and 33 were rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent 6,273,730 to Chang (hereinafter "Chang"), claims 9-11, 13, 21-23, and 25 were rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent 6,046,912 to Leman (hereinafter "Leman"), and claims 16-19, 28-31, and 36-39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Leman in view of Chang. Claims 3, 4, 12, 14, 15, 20, 24, 26, 27, 32, 34, and 35 were objected to as being dependent upon a rejected base claims, but were indicated as being allowable if rewritten in independent form. In a response dated April 22, 2002, the Applicant traversed all of the rejections. No amendments were proposed in this response.

In a Final Office Action mailed May 8, 2002, the Examiner maintained all of the rejections set forth in the Office Action of April 10, 2002. In an amendment under 37 C.F.R. § 1.116 dated June 13, 2002, the Applicant proposed to amend claims 1, 3, 5, 9, 14, 16, 21, 26, 28, and 33-37, and the Applicant proposed to add new claims 40-45. In an Advisory Action mailed July 3, 2002, the Examiner indicated that the proposed amendments would not be entered because new claims were presented without canceling a corresponding number of finally rejected claims.

On July 29, 2002, the Applicant filed Request for Continued Examination (RCE) along with a Preliminary Amendment. In this Preliminary Amendment, the Applicant proposed amendments to claims 1, 3, 5, 9, 14, 16, 21, 26, 28, and 33-37, and also proposed new claims 40-58. The amendments to claims 1, 3, 5, 9, 14, 16, 21, 26, 28, and 33-37, as well as new claims 40-45, set forth in the Preliminary Amendment were the same as that proposed in the response dated June 13, 2002.

In an Office Action mailed August 28, 2002, claims 1-3, 5-8, 33-35, and 40-46 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent 6,004,139 to Dramstad et al. (hereinafter "Dramstad"), and claims 9-14, 16-26, 28-32, 36-39, 48-50, and 52-58 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dramstad in view of Leman. Claims 4, 15, 27, and 51 were objected to as being dependent upon a rejected base claims, but were indicated as being allowable if rewritten in independent form. In a response dated October 9, 2002, the Applicant traversed all rejections set forth in the Office Action, but no amendments were proposed therein.

In a Final Office Action mailed December 4, 2002, the Examiner maintained all of the rejections set forth in the Office Action of August 28, 2002. In a response dated January 6, 2003, the Applicant again traversed all of the rejections set forth by the Examiner. In an Advisory Action mailed February 25, 2003, the Examiner again maintained all of the rejections. The Applicant filed a Notice of Appeal on January 6, 2003, which was received in the Patent Office on January 13, 2003.

In summary, claims 1-3, 5-8, 33-35, and 40-46 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Dramstad, and claims 9-14, 16-26, 28-32, 36-39, 48-50, and 52-58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dramstad in view of Leman. Claims 4, 15, 27, and 51 stand objected to.

As required by 37 C.F.R. § 1.192(c), Applicant has provided a copy of the currently pending claims in Appendix A. The claims presented in Appendix A include the amendments proposed by Applicant in the Preliminary Amendment that accompanied the RCE filed July 29, 2002.

(5) SUMMARY OF THE INVENTION

It is known in the art to couple a number of peripheral cards to a motherboard using a riser card that is inserted into a card connector on the motherboard, such that a desired form factor can be achieved. Specification, at 0008 (pg 4, lines 16-23). However, in the prior art, all signals for each peripheral card attached to the riser card must be routed through the card connector to which the riser card is connected and, therefore, a customized motherboard is necessary to accommodate the riser card and additional signal lines. Specification, at 0008 (pg 4, lines 24-29).

An example of a prior art customized motherboard and riser card assembly is illustrated in FIGS. 3 and 4. The motherboard assembly **200** includes a motherboard **205** having a plurality of card connectors **260**, each card connector for receiving a peripheral card **10**. Specification, at 0021, 0022 (pg 7, lines 4-6, 18-20). A riser card **280** is inserted into one of the card connectors **260** on motherboard **205**, and the riser card **280** has a number of secondary card connectors **283**. Specification, at 0023 (pg 7, lines 29-31; pg 8, lines 1-4). Coupled to each of the secondary card connectors **283** is a peripheral card **10**, wherein the riser card **280** orients the peripheral cards **10** substantially parallel to the motherboard **205** in a manner providing a relatively small form factor. Specification, at 0023 (pg 8, lines 1-10). However, to achieve the small form factor, the motherboard and at least one card connector **260** must be modified to receive the riser card **280**. Specification, at 0024 (pg 8, lines 11-23). More specifically, all signals directed to each peripheral card **10** secured on the riser card **280** must be routed to these peripheral cards through the single card connector **260** to which the riser card **280** is attached. *Id.* Thus, additional signal lines **262** and a supplemental connector **265** on the motherboard **205**

may be needed to adapt the motherboard **205** for use with the riser card **280**. *Id.* Such customized motherboards are undesirable due to the higher costs associated with the manufacture of non-standard motherboards. Specification, at 0026 (pg 9, lines 1-4).

Various embodiments of the invention, namely, a riser card assembly **380**, **480**, **580** providing a small form factor, yet usable with a standard motherboard assembly **100**, are illustrated in FIGS. 5 through 8. An embodiment of the standard motherboard assembly **100** is shown in FIG. 1.

With reference to FIG. 1, the standard motherboard assembly **100** comprises a motherboard **105** (e.g., an ATX compatible motherboard) including a processor **110**, a plurality of memory slots **120**, a power connector **130**, connectors **140** for hard disk and/or floppy disk drives, a number of I/O ports **150**, as well as chip set **170**. Specification, at 0018, 0019, 0027, 0028 (pg 5, line 5 through pg 6, line 21; pg 9, lines 5-24). Also disposed on the motherboard **105** is a plurality of card connectors **160**, each card connector adapted to receive a peripheral card (e.g., a PCI compatible peripheral card). Specification, at 0019, 0028 (pg 6, lines 13-21; pg 9, lines 15-24). Signal lines **162** disposed on motherboard **105** extend from each of the card connectors **160**, and these signal lines couple each card connector with the chip set **170**. *Id.* For example, a "REQ#" line **162a** and a "GNT#" line **162b** may couple each card connector **160** to the chip set **170**. *Id.* A signal line **162** may comprise either an electrical or optical communication path, or other communication path known in the art. Specification, at 0028 (pg 9, lines 22-24).

Turning to FIG. 5, a riser card assembly **380** couples one or more peripheral cards **10** to the motherboard **105**, and the riser card assembly **380** orients the peripheral cards

10 relative to the motherboard **105** in a configuration providing a small form factor. Specification, at 0029 (pg 9, lines 25-31). The riser card assembly **380** comprises a mounting portion **390** and a routing portion **395**, wherein the mounting portion is coupled to one of the card connectors **160** on motherboard **105**. *Id.*

The mounting portion **390** includes one or more secondary card connectors **393**, each secondary card connector capable of receiving a peripheral card **10**. Specification, at 0029 (pg 9, lines 27-31). In one embodiment, as illustrated in FIG. 5, the mounting portion **390** comprises a substantially vertical riser card inserted into a single card connector **160m** and having one secondary card connector **393** mounted on, or example, each opposing side of the vertical riser card. Specification, at 0029 (pg 9, line 31 through pg 10, line 5. The vertical riser and secondary card connectors **393** orient each of the peripheral cards **10** substantially parallel to the motherboard **105**. *Id.* The mounting portion **390** includes circuitry or other communications paths to couple the signal lines **162** received at its mating card connector **160m** to one of the secondary card connectors **393**. Specification, at 0031 (pg 10, lines 13-22).

The routing portion **395** is coupled to another one of the card connectors **160r** on motherboard **105**. Specification, at 0033 (pg 11, lines 3-7). In the embodiment of FIG. 5, the routing portion **395** comprises a riser **397** coupled to the card connector **160r** and another riser **398** coupling the riser **397** to mounting portion **390**. Specification, at 0034 (pg 11, lines 21-27). The routing portion **395** includes circuitry or other communication paths to couple the signal lines **162** received at its mating card connector **160r** to corresponding communication paths on the mounting portion **390**, and the corresponding communication paths on the mounting portion **390** route these signal lines to another one

of the secondary card connectors **393** on the mounting portion **390**. Specification, at 0033 (pg 11, lines 7-17).

The riser card assembly **380** of FIG. 5 is but one embodiment of such a riser card assembly. Each of the mounting portion **390** and routing portion **395** may have any other suitable structure or configuration and may be comprised of any suitable material(s). Specification, at 0032, 0034 (pg 10, line 23 through pg 11, line 2; pg 11, line 21 through pg 12, line 2. The mounting portion **390** and routing portion **395** may comprise separate parts that are interconnected by any suitable means or, in another embodiment, these two parts may comprise a single, integrated component. Specification, at 0035 (pg 12, lines 3-11). Also, the two risers **397**, **398** of routing portion **395** may comprise separate parts or, alternatively, a single integrated part. Specification, at 0034 (pg 11, lines 29-31). Other embodiments are shown in FIGS. 6 through 8, which are discussed below.

Referring to FIG. 6, a riser card assembly **480** includes a mounting portion **490** and two routing portions **495a**, **495b**. Specification, at 0037 (pg 12, lines 22-28). Therefore, riser card assembly **480** is capable of coupling three peripheral cards **10** to three separate card connectors **160**, respectively, on motherboard **105**. *Id.* FIG. 6 also illustrates another embodiment, wherein a routing portion **495b** comprises a flexible element (e.g., a flat ribbon cable). Specification, at 0037 (pg 12, lines 25-26).

Referring to FIG. 7, a riser card assembly **580** includes a mounting portion **590**, a first routing portion **595a**, and a second routing portion **595b**. Specification, at 0038 (pg 12, line 29 through pg 13, line 7). The first routing portion **595a** functions in a manner similar to that described above; however, the second routing portion **595b** comprises a compound routing portion. *Id.* The compound routing portion **595b** is connected with

two separate card connectors **160** on motherboard **105**. *Id.* Compound routing portion **595b** couples the signal lines received at each of its mating card connectors **160** to the mounting portion **590**, wherein the mounting portion **590** couples these signal lines to two separate secondary card connectors **593** disposed thereon. *Id.*

Referring to FIG. 8, the riser card assembly 380 and motherboard assembly 100 of FIG. 5 are shown disposed in the chassis 7 of a computer system 5. Specification, at 0039 (pg 13, lines 8-19). The computer system 5 also includes a number of other components (e.g., power supply 20, hard disk drive 30, floppy disk drive 40, CD ROM drive 50, and cooling fans 60) disposed within the chassis. *Id.*

In summary, the riser card assembly **380** (or **480**, **580**) secures one or more peripheral cards **10** to the motherboard **105** in a configuration providing a small form factor, yet not requiring a customized motherboard. The mounting portion **390** is secured in one card connector **160m** on the motherboard **105**, and the mounting portion **390** includes communication paths to route signal lines **162** received at its mating card connector **160m** to one secondary card connector **393** disposed thereon. The routing portion **395** is secured in a second card connector **160r** on motherboard **105**, and the routing portion **395** includes communications paths to route signal lines **162** received at its mating card connector **160r** to the mounting portion **390**, wherein the mounting portion **390** includes other communication paths to route these signal lines to another secondary card connector **393** disposed thereon. Thus, each secondary card connector **393** on mounting portion **390** – and, hence, each peripheral card **10** secured on mounting portion **390** – is ultimately coupled with one of the card connectors **160** on motherboard **105**. *See, e.g.*, Specification, at 0036, 0040 (pg 12, lines 12-21; pg 13, lines 20-28).

The disclosed embodiments may be better understood with reference to some of the claims. One of the disclosed embodiments is claimed in independent claim 1, which is reproduced below with reference numerals added from FIG. 5.

1. An apparatus comprising:

a mounting portion (390) including a first communication path to route at least one signal line from a first card connector (160m) on a circuit board (105) to a first card connector (393) on the mounting portion (390); and

a routing portion (395) including a communication path, the communication path of the routing portion (395) to route at least one signal line from a second card connector (160r) on the circuit board (105) to the mounting portion (390), a second communication path of the mounting portion (390) to route the at least one signal line of the second card connector (160r) on the circuit board (105) to a second card connector (393) on the mounting portion (390).

Another of the disclosed embodiments is claimed in independent claim 46, which is reproduced below with reference numerals added from FIGS. 1 and 5.

46. An apparatus comprising:

a circuit board (105);

a first card connector (160m) disposed on the circuit board (105) and having at least one signal line (162) extending therefrom;

a second card connector (160r) disposed on the circuit board (105) and having at least one signal line (162) extending therefrom;

a mounting portion (390) secured in the first card connector (160m) on the circuit board (105), the mounting portion (390) including a first communication path to couple the at least one signal line (162) of the first card connector (160m) on the circuit board (105) to a first card connector (393) disposed on the mounting portion (390); and

a routing portion (395) secured in the second card connector (160r) on the circuit board (105), the routing portion (395) including a communication path to couple the at least one signal line (162) of the second card connector (160r) on the circuit board (105) to the mounting portion (390), a second communication path of the mounting portion (390) to couple the at least one signal line (162) of the second card connector (160r) on the circuit board (105) to a second card connector (393) disposed on the mounting portion (390).

(6) ISSUES

A. Whether claims 1-3, 5-8, 33-35, and 40-46 are patentable over United States Patent 6,004,139 to Dramstad et al. under 35 U.S.C. § 102(b).

B. Whether claims 9-14, 16-26, 28-32, 36-39, 48-50, and 52-58 are patentable over Dramstad in view of United States Patent 6,046,912 to Leman under 35 U.S.C. § 103(a).

(7) GROUPING OF CLAIMS

The grouping of the claims is as follows:

(a) With respect to the first issue set forth above, claims 1-3, 5-8, 33-35, and 40-46 stand and fall together.

(b) With respect to the second issue set forth above, claims 9-14, 16-26, 28-32, 36-39, 48-50, and 52-58 stand and fall together.

The Applicant respectfully points out that claims 4, 15, 27, and 51 – each of which has been indicated to contain allowable subject matter – do not stand and fall with their respective independent claims. Applicant also respectfully notes that no basis for rejecting claim 47 has been set forth by the Examiner.

(8) ARGUMENT

The Examiner has maintained rejections under both 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a). As a respectful reminder, the applicable law for setting forth a rejection under each of §§ 102 and 103, respectively, is set forth below.

A claim is anticipated under 35 U.S.C. § 102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). See M.P.E.P. § 2131.

A proper rejection under 35 U.S.C. § 103(a) requires that the Patent Office must first establish a prima facie case of obviousness. M.P.E.P. § 2142. Three basic requirements must be shown to establish a prima facie case of obviousness. M.P.E.P. §§ 2142 and 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. M.P.E.P. § 2143.01. Second, there must be a reasonable expectation of success. M.P.E.P. § 2143.02. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. M.P.E.P. § 2143.03.

(A) Patentability of Claims 1-3, 5-8, 33-35, and 40-46

Independent claim 1, which Applicant asserts to be the broadest claim currently pending in the application, recites:

1. An apparatus comprising:

a mounting portion including a first communication path to route at least one signal line from a first card connector on a circuit board to a first card connector on the mounting portion; and

a routing portion including a communication path, the communication path of the routing portion to route at least one signal line from a second card connector on the circuit board to the mounting portion, a second communication path of the mounting portion to route the at least one signal line of the second card connector on the circuit board to a second card connector on the mounting portion.

The first element of claim 1 is a "mounting portion". The mounting portion includes "a first card connector" and "a second card connector" disposed thereon. The mounting portion is further defined by the limitations of "a first communication path" and "a second communication path". Note, however, that each of the first and second communication paths on the mounting portion are further limited. More specifically, the first communication path is "to route at least one signal line from a first card connector on a circuit board to" the first card connector of the mounting portion, and the second communication path is "to route the at least one signal line of the second card connector on the circuit board to" the second card connector of the mounting portion.

The second element of claim 1 is a "routing portion". The routing portion includes "a communication path", and this communication path is further limited in the claim. In particular, the communication path of the routing portion is "to route at least one signal line from a second card connector on the circuit board to" the mounting portion. As noted above, it is then the second communication path of the mounting

portion that routes the signal line of the second circuit board card connector to the second card connector of the mounting portion.

In summary, claim 1 recites the following limitations (in outline form with reference numerals from FIG. 5 added in parentheses for ease of understanding):

I. Mounting portion (390)
  A. First card connector (393)
  B. Second card connector (393)
  C. First communication path
    (i) To route a signal line of a first circuit board card connector (160m) to the first card connector (393) on the mounting portion (390)
  D. Second communication path
    (ii) To route a signal line of the second circuit board card connector (160r) to the second card connector (393) of the mounting portion (390), wherein this signal line is routed to the mounting portion (390) by the communication path of the routing portion (395), as noted below in II(A)(i)

II. Routing portion (395)
  A. Communication path
    (i) To route a signal line of a second circuit board card connector (160r) to the mounting portion (390).

Each of independent claims 9, 21, 33, 36, and 46 recites limitations similar to the above-noted limitations of claim 1.

Each of independent claims 1, 33, and 46 stand rejected under 35 U.S.C. § 102(b) based upon United States Patent 6,004,139 to Dramstad et al. (hereinafter "Dramstad"). Although addressed in Section (8)(B) below, it is also noted here that each of

independent claims 9, 21, and 36 is rejected under 35 U.S.C. § 103(a) based upon Dramstad in view of United States Patent 6,046,912 to Leman (hereinafter "Leman").

Dramstad is directed to a memory card adapter enabling a system equipped with older 30-pin SIMMs (Single In-Line Memory Modules) to accept newer 72-pin SIMMs and to a memory card adaptor enabling a system equipped for accepting SIMMs to accept DIMMs (Dual In-Line Memory Modules). Dramstad, at Column 1, Lines 31-43; Column 2, Lines 7-17. The memory card adaptor is plugged into a plurality of SIMM sockets, thereby enabling a DIMM (or a 72-pin SIMM) coupled with the adaptor to emulate a plurality of SIMMs and permitting older computer systems to utilize newer memory expansion cards. Dramstad, at Column 2, Lines 27-46.

In one embodiment disclosed in FIG. 6 of Dramstad, a memory card adaptor **50** has a DIMM socket **51** mounted thereto, and the memory card adaptor **50** is coupled with a motherboard **54** having two SIMM sockets **52, 53** disposed thereon. Dramstad, at Column 5, Lines 1-4. The DIMM socket **51** on adaptor card **50** is electrically coupled to one of the SIMM sockets (i.e., socket **52**) via electrical conductors **59a** in the adaptor card **50** itself. Dramstad, at Column 5, Lines 21-30. The DIMM socket **51** is electrically coupled to the other of the SIMM sockets (i.e., socket **53**) via a ribbon cable **58** and electrical conductors **59** in the adaptor card **50**. Dramstad, at Column 5, Lines 12-20 and 31-34. **Therefore, both SIMM sockets 52, 53 on motherboard 54 are coupled to the same DIMM socket 51 on the adaptor card 50.**

In another embodiment disclosed in FIG. 7 of Dramstad, a memory card adaptor **66** having a 72-pin SIMM socket **60** is coupled to a motherboard **61** having four 30-pin SIMM sockets **62, 63, 64, 65** mounted thereon. Dramstad, at Column 5, Lines 35-42.

The 72-pin SIMM socket **60** is coupled to a first of the 30-pin SIMMs (i.e., socket **62**) via electrical conductors **81** on the adaptor card **66** itself. Dramstad, at Column 5, Lines 42-45 and 55-59. The 72-pin SIMM socket **60** is coupled to a second of the 30-pin SIMMs (i.e., socket **63**) via a ribbon cable **70** and electrical conductors **82** in the adaptor card **66**. Dramstad, at Column 5, Lines 46-54 and 60-63. Similarly, the 72-pin SIMM socket **60** is coupled to a third of the 30-pin SIMMs (i.e., socket **64**) via a ribbon cable **71** and electrical conductors **82**, whereas the 72-pin SIMM socket **60** is coupled to a fourth of the 30-pin SIMMs (i.e., socket **65**) via a ribbon cable **72** and electrical conductors **82**. Dramstad, at Column 5, Lines 46-54 and 60-63. **Thus, all four 30-pin SIMM sockets 62, 63, 64, 65 on motherboard 61 are coupled to the same 72-pin SIMM socket 60 on adaptor card 66.**

Thus, for all embodiments disclosed in Dramstad, **all sockets** on the motherboard are **coupled to the same socket** on the adaptor card, and the Examiner has not identified any language or teaching in Dramstad to the contrary. Note that, in FIG. 7, the connectors **67**, **68**, **69** on adaptor card **66** are simply for receiving the ribbon cables **70**, **71**, **72**, respectively, and these connectors are not for receiving a memory module (e.g., a 72-pin SIMM or a DIMM) or other expansion card. Similarly, in FIG. 6 of Dramstad, the connector **55** on adaptor card **50** is for receiving ribbon cable **58** and not for receiving a memory module or expansion card.

In contrast to the structure disclosed in Dramstad, claim 1 in this application recites (and independent claims 9, 21, 33, 36, and 46 recite similar limitations, as noted above) an apparatus that couples a first card connector on a circuit board to a first card connector on a mounting portion and, further, that couples a second card connector on the

circuit board to a second card connector on the mounting portion. Dramstad does not disclose such an apparatus. Rather, as described above, Dramstad discloses a structure for coupling a number of sockets on a motherboard to the same, individual socket on an adaptor card. It follows, therefore, the Dramstad fails to disclose at least the limitation of "a second communication path" on the mounting portion that is "to route the at least one signal line of the second card connector on the circuit board to a second card connector on the mounting portion."

To overcome the lack of disclosure in Dramstad, the Examiner as adopted a very broad interpretation of independent claim 1 (as well as the other independent claims). In the Final Office Action mailed December 4, 2002 (at page 18), the Examiner states:

> The Examiner also points out that a "mounting portion" in an apparatus ***is determined to mean, "a portion or surface that something (in the instance case, a card connector) can be mounted on***, and a "routing portion" in an apparatus ***is determined to mean, "an element or device that is used to route something (in the instant case, electric signals) from one place to another.*** Dramstad et al at least shows these limitations (refer to the elements and Figures as outlined above.

The Examiner's interpretation of the mounting portion and routing portion elements recited in the independent claims wholly ignores express limitations recited in each of these claims. Furthermore, it would seem the Examiner arrived at the proffered definitions of the mounting portion and routing portion elements without regard for the express claim language or the written description. As noted above, the **routing portion** includes a **communication path** to route a signal line of a second circuit board card connector to the mounting portion. The **mounting portion** includes a **first card connector**, a **second card connector**, a **first communication path** to route a signal line of a first circuit board card connector to the first card connector on the mounting portion,

and a **second communication path** to route the signal line associated with the second circuit board card connector (this signal having been routed to the mounting portion by the communication path of the routing portion) to the second card connector on the mounting portion. As noted above, Dramstad does not disclose all of these limitations.

It is respectfully asserted that the Examiner's interpretation of the claims, as described above, is overly broad, is not supported by the Applicant's written description, and is inconsistent with applicable law. Further, it is respectfully asserted that without such a broad interpretation of the claims, the claims are allowable over the cited art.

While it is understood that claims must be given their broadest, reasonable interpretation during examination – see M.P.E.P. § 2111 – this rule of claim interpretation is not without limitation. For example, an anticipation rejection under 35 U.S.C. § 102 can only be maintained if ***each and every limitation*** recited in a claim is found in a single prior art reference. See M.P.E.P. § 2131. Similarly, to establish a prima facie case of obviousness under 35 U.S.C. § 103, a prior art reference or combination of references must teach or suggest ***all of the limitations*** of a claim. See M.P.E.P. § 2143. Thus, it is inconsistent with applicable law for the Examiner to completely ignore any express claim limitation, an action the Examiner has taken with respect to the above-mentioned independent claims.

The Examiner's broad interpretation of the claims is also inconsistent with, and unsupported by, the Applicant's written description. Paragraphs 0029, 0031, and 0033 of the as-filed specification, which describe one embodiment of the invention, provide:

> [0029] A riser card assembly 380 couples one or more peripheral cards 10 to the motherboard 105. The riser card assembly 380 comprises a mounting portion 390 and a routing portion 395. The ***mounting portion 390*** is coupled to

any one of the card connectors 160 on circuit board 105 and ***includes one or more secondary card connectors 393***, each secondary card connector 393 for receiving a peripheral card 10 and orienting that peripheral card 10 relative to the motherboard 105 in a configuration providing a small form factor. By way of example, as illustrated in FIG. 5, the mounting portion 390 may comprise a substantially vertical riser card inserted into a card connector designated 160m and having two secondary card connectors 393 secured thereto – one secondary card connector 393 mounted on each of opposing sides of the vertical riser card. ***Each secondary card connector 393 is adapted to receive a peripheral card 10*** and to orient that peripheral card 10 substantially parallel to the motherboard 105.

[0031] The ***mounting portion 390 includes circuitry or other communication paths to couple the signal lines 162 received at its mating card connector 160m to one of the secondary card connectors 393***. Thus, one peripheral card 10 attached to mounting portion 390 will receive signals – i.e., REQ#, GNT#, PCI CLK, interrupt requests, address and data signals, and transaction control signals – from chip set 170 via the card connector 160m and mounting portion 390. For example, the mounting portion 390 may include circuitry to couple at least a REQ# line 162a and a GNT# line 162b from the card connector 160m to one peripheral card 10, as well as its mating secondary connector 393. All other peripheral cards 10 attached to mounting portion 390 are coupled to the chip set 170 via the routing portion 395, as will be explained in greater detail below.

[0033] As noted above, the mounting portion 390 couples (via circuitry on mounting portion 390 and signal lines 162 at its mating card connector 160m) only one peripheral card 10 to the chip set 170. The routing portion 395 routes all of the signal lines 162 – or a selected portion thereof – coupled to an adjacent card connector 160r from that card connector 160r to the mounting portion 390. The ***routing portion 395 includes circuitry or other communication paths to couple the signal lines 162 received at its mating card connector 160r to corresponding communication paths on the mounting portion 390***, the ***mounting portion 390, in turn, routing these corresponding communication paths to another one of the secondary card connectors 393 mounted thereon***. Thus, a second peripheral card 10 may be attached to mounting portion 390, and this peripheral card will receive signals from chip set 170 via the card connector 160r, routing portion 395, and mounting portion 390. For example, the routing portion 395, as well as the mounting portion 390, may each include circuitry to couple at least a REQ# line 162a and a GNT# line 162b from the card connector 160r to the second peripheral card 10 and its mating secondary connector 393. It should be understood that the card connector 160r (receiving routing portion 395) and the card connector 160m (receiving mounting portion 390) do not necessarily lie directly adjacent to one another but, rather, may be separated by one or more intervening card connectors 160.

In view of the paragraphs of the written description reproduced above, it is apparent that the Examiner has failed to examine the written description and give the claims their broadest, reasonable interpretation that is consistent with the specification.

See *In re Morris*, 44 U.S.P.Q.2d 1023, 1027 (Fed. Cir. 1997) (stating that "it would be unreasonable for the PTO to ignore any interpretive guidance afforded by the applicant's written description"); *Rowe v. Dror*, 42 U.S.P.Q.2d 1550, 1555 (Fed. Cir. 1997) (stating that "claims receive their broadest reasonable meaning" during the examination process, but this "does not relieve the PTO of its essential task of examining the entire patent disclosure to discern the meaning of claims words and phrases"); and *In re Sneed and Young*, 218 U.S.P.Q. 385, 388 (Fed. Cir. 1983) (stating that it "is axiomatic that, in proceedings before the PTO, claims in an application are to be given their broadest reasonable interpretation **consistent with** the specification") (emphasis added).

In summary, when each independent claim of the application is given an interpretation consistent with the specification and that accounts for all express claim limitations, Dramstad fails to disclose all limitations of any independent claim. Thus, independent claims 1, 33, and 46 are novel in view of Dramstad (as are independent claims 9, 21, and 36). Also, claims 2, 3, 5-8, 40, and 41 are allowable as depending from novel, independent claim 1, and claims 34-35 are allowable as depending from novel, independent claim 33. It is further noted that claims 42-43 and claims 44-45 are allowable as depending from novel, independent claims 9 and 21, respectively.

(B) Patentability of Claims 9-14, 16-26, 28-32, 36-39, 48-50, and 52-58

As previously noted, claim 9-14, 16-26, 28-32, 36-39, 48-50, and 52-58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dramstad in view of Leman.

The disclosure of Dramstad is summarized above. Leman discloses a motherboard **300** having an attached riser board **304**. Leman, at Column 2, Lines 43-45; FIG. 3. An adapter **302** couples a PCI bus on motherboard **300** to a PCI bus on riser board **304**, the adapter **302** coupled between a PCI connector **306** on motherboard **300** and a connector **308** on riser board **304**. Leman, at Column 2, Lines 44-48. The riser board provides one or more connectors **310** for receiving PCI add-in cards oriented substantially parallel to the motherboard **300**. Leman, at Column 2, Lines 48-52. In another embodiment of the Leman patent, a riser board **500** is directly connected to the PCI slot **306** on motherboard **300**, and an adapter (e.g., adapter **302** of FIG. 3) is not necessary. Leman, at Column 3, Lines 15-18; FIG. 5.

In the embodiment of FIG. 3 of Leman, the adapter **302** is inserted into the PCI slot **306**, and the riser board **304** is mechanically attached to the motherboard **300**. The riser board **304** is not inserted or otherwise coupled with a PCI slot on the motherboard **300** (see FIG. 3 and accompanying text). In the embodiment of FIG. 5, the riser board **500** is shown inserted into the PCI slot **306** on motherboard **300**, and the embodiment of FIG. 5 does not include an adapter **302**. Thus, for either of the embodiments of FIGS. 3 and 5, respectively, all signals to the plurality of card connectors **310** on riser board **304** (or **500**) are routed from a single PCI slot **306** on the motherboard **300**.

As set forth above in Section (A), Dramstad fails to disclose at least the limitation of "a second communication path" on the mounting portion that is "to route the at least one signal line of the second card connector on the circuit board to a second card connector on the mounting portion." Leman also fails to disclose at least this limitation. Note that, in Leman, all card connectors **310** on the riser card **304** (or **500**) are ultimately

coupled with a single card connector **306** on the motherboard **300**. Thus, the structure disclosed in Leman would not route a signal line from "a second card connector" on the motherboard and, further, would not include any communication path to do so.

Also, it is respectfully pointed out that either embodiment (FIG. 3 or FIG. 5) of the Leman patent discloses one problem identified in the prior art that the claims of the present invention overcome. More specifically, either embodiment disclosed in Leman would require a customized motherboard to route all signals through the single PCI card slot **306** to which the adapter **302** of FIG. 3, or the riser board **500** of FIG. 5, is coupled. Avoiding the use of customized motherboards by eliminating the need for routing additional signal paths through a single card slot is one problem the present invention overcomes. Specification, at 0008 and 0024 (pg 4, lines 22-29; pg 8, lines 11-23).

In summary, Dramstad and Leman, either individually or in combination, fail to disclose at least the above-noted limitations of the independent claims. Thus, each of independent claims 9, 21, and 36 (as well as independent claim 46) is nonobvious in view of the combination of Dramstad and Leman.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. §2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 10-14 and 16-20 are allowable as depending from nonobvious, independent claim 9, claims 22-26 and 28-32 are allowable as depending from nonobvious, independent claim 21, and claims 37-39 are allowable as depending from nonobvious, independent claim 36. Further, it is noted that claims 48-50 and 52-58 are allowable as depending from nonobvious, independent claim 46.

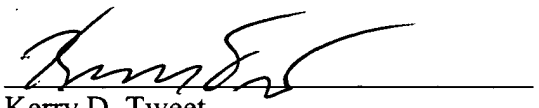
(9) APPENDIX

A copy of claims 1-58 is appended hereto as "Appendix A."

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, L.L.P.

Date: March 6, 2003



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APPENDIX A:

1. (Amended) An apparatus comprising:
a mounting portion including a first communication path to route at least one signal line from a first card connector on a circuit board to a first card connector on the mounting portion; and
a routing portion including a communication path, the communication path of the routing portion to route at least one signal line from a second card connector on the circuit board to the mounting portion, a second communication path of the mounting portion to route the at least one signal line of the second card connector on the circuit board to a second card connector on the mounting portion.

2. The apparatus of claim 1, the mounting portion and the routing portion comprising a single integrated component.

3. (Amended) The apparatus of claim 1, further comprising at least one other routing portion including a communication path to route at least one signal line from a third card connector on the circuit board to the mounting portion, a third communication path of the mounting portion to route the at least one signal line of the third card connector on the circuit board to a third card connector on the mounting portion.

4. The apparatus of claim 3, the routing portion and the at least one other routing portion comprising a compound routing portion.

5. (Amended) The apparatus of claim 1, the routing portion comprising:
a first riser for coupling with the second card connector on the circuit board; and
a second riser coupled with the first riser, the second riser for coupling with the mounting portion.

6. The apparatus of claim 5, the first riser and the second riser comprising a single part.

7. The apparatus of claim 5, the first riser oriented substantially transverse to the circuit board and the second riser oriented substantially parallel to the circuit board.

8. The apparatus of claim 1, the routing portion comprising a flexible cable.

9. (Amended) An apparatus comprising:
a circuit board;
a processor disposed on the circuit board;
a chip set disposed on the circuit board and coupled to the processor;
a first card connector disposed on the circuit board and coupled to the chip set by at least one signal line;
a second card connector disposed on the circuit board and coupled to the chip set by at least one signal line;
a mounting portion secured in the first card connector on the circuit board, the mounting portion including a first communication path to couple the at least one signal line of the first card connector on the circuit board to a first card connector disposed on the mounting portion; and
a routing portion secured in the second card connector on the circuit board, the routing portion including a communication path to couple the at least one signal line of the second card connector on the circuit board to the mounting portion, a second communication path of the mounting portion to couple the at least one signal line of the second card connector on the circuit board to a second card connector disposed on the mounting portion.

10. The apparatus of claim 9, further comprising a peripheral card secured in one of the first card connector on the mounting portion and the second card connector on the mounting portion.

11. The apparatus of claim 10, the mounting portion to orient the peripheral card substantially parallel to the circuit board.

12. The apparatus of claim 9, each of the at least one signal line of the first card connector on the circuit board and the at least one signal line of the second card connector on the circuit board comprising at least a REQ# line and a GNT# line.

13. The apparatus of claim 9, the mounting portion and the routing portion comprising a single integrated component.

14. (Amended) The apparatus of claim 9, further comprising:
a third card connector disposed on the circuit board and coupled to the chip set by at least one signal line; and
at least one other routing portion secured in the third card connector on the circuit board, the at least one other routing portion including a communication path to couple the at least one signal line of the third card connector on the circuit board to the mounting portion, a third communication path of the mounting portion to couple the at least one signal line of the third card connector on the circuit board to a third card connector disposed on the mounting portion.

15. The apparatus of claim 14, the routing portion and the at least one other routing portion comprising a compound routing portion.

16. (Amended) The apparatus of claim 9, the routing portion comprising:
a first riser coupled with the second card connector on the circuit board; and
a second riser coupled with the first riser, the second riser coupled with the mounting portion.

17. The apparatus of claim 16, the first riser and the second riser comprising a single part.

18. The apparatus of claim 16, the first riser oriented substantially transverse to the circuit board and the second riser oriented substantially parallel to the circuit board.

19. The apparatus of claim 9, the routing portion comprising a flexible cable.

20. The apparatus of claim 9, the first card connector on the circuit board separated from the second card connector on the circuit board by at least one intervening card connector disposed on the circuit board.

21. (Amended) An apparatus comprising:

a chassis;

a circuit board disposed in the chassis;

a processor disposed on the circuit board;

a chip set disposed on the circuit board and coupled to the processor;

a first card connector disposed on the circuit board and coupled to the chip set by at least one signal line;

a second card connector disposed on the circuit board and coupled to the chip set by at least one signal line;

a mounting portion secured in the first card connector on the circuit board, the mounting portion including a first communication path to couple the at least one signal line of the first card connector on the circuit board to a first card connector disposed on the mounting portion; and

a routing portion secured in the second card connector on the circuit board, the routing portion including a communication path to couple the at least one signal line of the second card connector on the circuit board to the mounting portion, a second communication path of the mounting portion to couple the at least one signal line of the second card connector on the circuit board to a second card connector disposed on the mounting portion.

22. The apparatus of claim 21, further comprising a peripheral card secured in one of the first card connector on the mounting portion and the second card connector on the mounting portion.

23. The apparatus of claim 22, the mounting portion to orient the peripheral card substantially parallel to the circuit board.

24. The apparatus of claim 21, each of the at least one signal line of the first card connector on the circuit board and the at least one signal line of the second card connector on the circuit board comprising at least a REQ# line and a GNT# line.

25. The apparatus of claim 21, the mounting portion and the routing portion comprising a single integrated component.

26. (Amended) The apparatus of claim 21, further comprising:
a third card connector disposed on the circuit board and coupled to the chip set by at least one signal line; and
at least one other routing portion secured in the third card connector on the circuit board, the at least one other routing portion including a communication path to couple the at least one signal line of the third card connector on the circuit board to the mounting portion, a third communication path of the mounting portion to couple the at least one signal line of the third card connector on the circuit board to a third card connector disposed on the mounting portion.

27. The apparatus of claim 26, the routing portion and the at least one other routing portion comprising a compound routing portion.

28. (Amended) The apparatus of claim 21, the routing portion comprising:
a first riser coupled with the second card connector on the circuit board; and
a second riser coupled with the first riser, the second riser coupled with the mounting portion.

29. The apparatus of claim 28, the first riser and the second riser comprising a single part.

30. The apparatus of claim 28, the first riser oriented substantially transverse to the circuit board and the second riser oriented substantially parallel to the circuit board.

31. The apparatus of claim 21, the routing portion comprising a flexible cable.

32. The apparatus of claim 21, the first card connector on the circuit board separated from the second card connector on the circuit board by at least one intervening card connector disposed on the circuit board.

33. (Amended) An apparatus comprising:
first routing means including a first communication means for routing at least one signal line from a first card connector on a circuit board to a first card connector disposed on the first routing means; and
second routing means including a communication means, the communication means of the second routing means for routing at least one signal line from a second card connector on the circuit board to the first routing means, a second communication means of the first routing means to route the at least one signal line of the second card connector on the circuit board to a second card connector disposed on the first routing means.

34. (Amended) The apparatus of claim 33, further comprising a third routing means including a communication means for routing at least one signal line from a third card connector on the circuit board to the first routing means, a third communication means of the first routing means to route the at least one signal line of the third card connector on the circuit board to a third card connector disposed on the first routing means.

35. (Amended) The apparatus of claim 33, each of the first and second communication means of the first routing means and the communication means of the second routing means to route one of an electrical signal and an optical signal.

36. (Amended) A method comprising:
securing a mounting structure to a first card connector on a circuit board;
securing a routing structure to a second card connector on the circuit board;
routing at least one signal line from the first card connector on the circuit board through a first communication path of the mounting structure to a first card connector on the mounting structure;
routing at least one signal line from the second card connector on the circuit board through a communication path of the routing structure to the mounting structure; and
routing the at least one signal line of the circuit board second card connector through a second communication path of the mounting structure to a second card connector on the mounting structure.

37. (Amended) The method of claim 36, further comprising:
securing a second routing structure in a third card connector on the circuit board;
routing at least one signal line from the third card connector on the circuit board through a communication path of the second routing structure to the mounting structure; and
routing the at least one signal line of the circuit board third card connector through a third communication path of the mounting structure to a third card connector on the mounting structure.

38. The method of claim 36, further comprising:
routing at least a REQ# line and a GNT# line from the first card connector on the circuit board to the first card connector on the mounting structure; and
routing at least a REQ# line and a GNT# line from the second card connector on the circuit board to the second card connector on the mounting structure.

39. The method of claim 36, further comprising securing a peripheral card in one of the first card connector on the mounting structure and the second card connector on the mounting structure.

40. The apparatus of claim 1, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an electrically conductive path.

41. The apparatus of claim 1, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an optical path.

42. The apparatus of claim 9, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an electrically conductive path.

43. The apparatus of claim 9, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an optical path.

44. The apparatus of claim 21, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an electrically conductive path.

45. The apparatus of claim 21, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an optical path.

46. An apparatus comprising:

a circuit board;

a first card connector disposed on the circuit board and having at least one signal line extending therefrom;

a second card connector disposed on the circuit board and having at least one signal line extending therefrom;

a mounting portion secured in the first card connector on the circuit board, the mounting portion including a first communication path to couple the at least one signal line of the first card connector on the circuit board to a first card connector disposed on the mounting portion; and

a routing portion secured in the second card connector on the circuit board, the routing portion including a communication path to couple the at least one signal line of the second card connector on the circuit board to the mounting portion, a second communication path of the mounting portion to couple the at least one signal line of the second card connector on the circuit board to a second card connector disposed on the mounting portion.

47. The apparatus of claim 46, further comprising a peripheral card secured in one of the first card connector on the mounting portion and the second card connector on the mounting portion.

48. The apparatus of claim 47, the mounting portion to orient the peripheral card substantially parallel to the circuit board.

49. The apparatus of claim 46, the mounting portion and the routing portion comprising a single integrated component.

50. The apparatus of claim 46, further comprising:
a third card connector disposed on the circuit board and having at least one signal line extending therefrom; and
at least one other routing portion secured in the third card connector on the circuit board, the at least one other routing portion including a communication path to couple the at least one signal line of the third card connector on the circuit board to the mounting portion, a third communication path of the mounting portion to couple the at least one signal line of the third card connector on the circuit board to a third card connector disposed on the mounting portion.

51. The apparatus of claim 50, the routing portion and the at least one other routing portion comprising a compound routing portion.

52. The apparatus of claim 46, the routing portion comprising:
a first riser coupled with the second card connector on the circuit board; and
a second riser coupled with the first riser, the second riser coupled with the mounting portion.

53. The apparatus of claim 52, the first riser and the second riser comprising a single part.

54. The apparatus of claim 52, the first riser oriented substantially transverse to the circuit board and the second riser oriented substantially parallel to the circuit board.

55. The apparatus of claim 46, the routing portion comprising a flexible cable.

56. The apparatus of claim 46, the first card connector on the circuit board separated from the second card connector on the circuit board by at least one intervening card connector disposed on the circuit board.

57. The apparatus of claim 46, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an electrically conductive path.

58. The apparatus of claim 46, wherein each of the first and second communication paths of the mounting portion and the communication path of the routing portion comprises an optical path.